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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,241	04/22/2004	Nobuyuki Endo	031794-14	7227

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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 05/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,241	ENDO, NOBUYUKI	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement received April 22, 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Information Disclosure Statement is being considered by the examiner.

Claim Objections

2. Claim 16 is objected to because of the following informalities:

In claim 16, line 2, it appears the language "the arbitration circuits prioritizes" should be changed to "the arbitration circuit prioritizes". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 7, 9, 11-13, 17 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Hatae et al (US PGPub No. 20020184471).

For claim 1, Hatae discloses a semiconductor integrated circuit (a semiconductor integrated circuit, par. 0001) comprising:

a central processing unit (the data processor includes a central processing unit, par. 0054);

a main memory control unit for controlling a main memory (a data transfer controller to control transfer of data for the data buffer, par. 0030);

an I/O channel control unit for controlling a peripheral device (a data input/output circuit, par. 0062; figs. 2, 3);

a first bus for connecting the central processing unit, main memory control unit and I/O channel control unit to each other (a first bus connecting the data buffer to the single instruction multiple data unit, par. 0014; the data access via the first data bus is controlled by the CPU via a CPU address bus and a control bus, par. 0056; data is fed to the data bus of the image memory and is then delivered to the data input/output circuit, par. 0070; fig. 2);

a local memory for storing information (a data buffer includes a high-speed memory such as a static RAM, par. 0013);

a second bus for connecting the local memory to the central processing unit; access control means for accessing the local memory in response to a request from outside (the data buffer includes a dual-port unit including a first port and a second port, the first port being connected via a first bus to a single instruction multiple data unit capable of conduction a concurrent operation for a plurality of data items, the second port being connected via a second bus to a data transfer control unit for controller

transfer of data for the data buffer, par. 0012-0014; image memory transferred to the data buffer is fed to the single instruction multiple data unit and is processed, par. 0013); and

a third bus for connecting the access control means to the local memory (the data transfer controller is connected via a third data bus and a third address bus to the image memory, par. 0057).

For claim 2, Hatae discloses the local memory includes a first access port connected to the second bus and a second access port connected to the third bus (a dual-port RAM including a first and second port; the first port is connected to the CPU address bus and the data bus to receive an access control signal from the CPU, the second port is connected to the data transfer controller to receive an access control signal from an address controller, par. 0064).

Claim 3 is rejected using the same rationale as for the rejection of claim 2 above.

For claim 7, Hatae discloses the local memory is RAM with an access port on one side (two-side buffer RAM arranged with a selector circuit and data bus, par. 0083; fig. 2, items 9, 9A, 9B).

For claim 9, Hatae discloses the local memory has a smaller capacity than the main memory but has a higher access speed than the main memory (the image memory includes a large-capacity, low-speed memory such as a dynamic RAM and synchronous DRAM, and the data buffer includes a high-speed memory such as a static RAM, par. 0013; fig. 1, items 9 and 17).

Claim 11 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 12 is rejected using the same rationale as for the rejection of claim 2 above.

Claim 13 is rejected using the same rationale as for the rejection of claim 3 above.

Claim 17 is rejected using the same rationale as for the rejection of claim 7 above.

Claim 19 is rejected using the same rationale as for the rejection of claim 9 above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4-6, 8, 14-16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatae et al (US PGPub No. 20020184471) and Fukunaga et al (US Patent No. 4,523,272).

For claim 4, Hatae discloses the invention as per rejection of claim 1 above.

Hatae fails to disclose the limitations of the current claim.

Fukunaga, however, helps disclose selection means connected between the second and third buses and the local memory for selecting the second bus or the third bus so as to connect the selected bus to the local memory (a bus selection control for a data transmission apparatus having at least one memory unit and a plurality of processors connected through a common bus for transmitting data between the memory unit and the processors and between the processors, col. 1, lines 6-12; a selection control system may be a distributed system in which bus selection control circuits are distributed in the processors and the memory unit, col. 3, lines 38-41; when any of the processors issues a bus selection request, it selects an address bus, data bus, or answer bus depending on whether the content of the request relates to a data write, data read, or answer to either of these, col. 2, lines 4-9).

Hatae and Fukunaga are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include selection means for selecting buses because this would aid in an improved bus throughput, particularly in a distributed function multiprocessor system, and reduce the number of total bus selection lines without reducing bus throughput (col. 1, lines 49-60), as taught by Fukunaga.

For claim 5, the combined teachings of Hatae and Fukunaga disclose the invention as per rejection of claim 4 above.

Fukunaga further helps disclose arbitration means for issuing an instruction to the selection means regarding selection of the second or third bus, on the basis of a

request to access the local memory from the central processing unit and a request to access the local memory from the access control means (when any of the processors issues a bus selection request, it selects an address bus, data bus, or answer bus depending on whether the content of the request relates to a data write, data read, or answer to either of these, col. 2, lines 4-9).

For claim 6, the combined teachings of Hatae and Fukunaga disclose the invention as per rejection of claim 5 above.

Fukunaga further helps disclose the arbitration means prioritizes the access request from the central processing unit over the access request from the access control means (the selection control circuit receives the request signals by request signal receivers and accepts only the request from the unit having a higher priority than that imparted to its own unit, and output signals of the request signal receivers are examined by a priority circuit to check to see if the request is from the higher priority unit or not, col. 4, lines 7-14; processors and the memory unit also issue request signals which are sent to the selection control circuit, col. 4, lines 1-3).

Claim 8 is rejected using the same rationale as for the rejection of claim 6 above.

Claim 14 is rejected using the same rationale as for the rejection of claim 4 above.

Claim 15 is rejected using the same rationale as for the rejection of claim 5 above.

Claim 16 is rejected using the same rationale as for the rejection of claim 6 above.

Claim 18 is rejected using the same rationale as for the rejection of claim 8 above.

7. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatae et al (US PGPub No. 20020184471), Fukunaga et al (US Patent No. 4,523,272) and Hadwiger et al (US PGPub No. 20040049293).

For claim 10, the combined teachings of Hatae and Fukunaga disclose the invention as per rejection of claim 5 above.

These teachings fail to disclose the limitations of the current claim.

Hadwiger et al (US PGPub No. 20040049293), however, helps disclose the arbitration means generates and issues a selection result signal, which indicates the selected bus, to the outside (each arbitration unit grants access to its bus, and an active bus select signal from a requestor to the arbitration unit indicates a request for access and arbitration, the arbitration unit either returns a wait signal for delaying access or grants the access, par. 0044).

Hatae, Fukunaga and Hadwiger are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a selection result signal because this would allow the bus arbitration module to selectively interconnect buses, so that there is no blocking or bandwidth starvation (abstract), as taught by Hadwiger.

Claim 20 is rejected using the same rationale as for the rejection of claim 10 above.

Citation of Pertinent Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Miwa et al (US Patent No. 5,581,698) discloses a semiconductor integrated circuit device including a direct memory access controller and an interface with an outside through an input/output circuit.

Brown (US PGPub No. 20030172225) discloses a virtual multiple port memory device including a random access memory having only one access port, multiple bus connection ports, and an arbiter for selectively granting to one of the bus connection ports access to the only access port.

Emerson et al (US PGPub No. 20040064646) discloses a memory controller system including a plurality of system buses, a multi-port memory controller, a plurality of system bus ports and a memory port, and selection of which bus interface circuit gets access to the memory controller.

Contact Information

9. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If

attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

5-4-06

PIERRE VITAL
PRIMARY EXAMINER